IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Pentakota	Docket No:	TI-37302
Serial No:	10/775,022	Examiner:	Wells, Kenneth
Filed:	2/9/2004	Art Unit:	2816
For:	OUTPUT BUFFER (as amended)		

APPEAL BRIEF PURSUANT TO 1.192(c)

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 571-273-8300 on 2-13-06.

Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the final Office Action mailed August 5, 2005, and the Advisory Action mailed November 8, 2005.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-5 were originally filed, and no claims have been cancelled or added.

However, Claims 4 and 5 have been indicated as allowable.

Consequently, the subject matter of the instant appeal is the final rejection of Claims 1-3.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1-5.

A Response After Final was filed on November 1, 2005.

The Advisory Action indicated that the response has been considered and Applicants presume that it has been entered.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Figure 1 shows the overall structure of a low noise output buffer 10 for a single data line. A high-bandwidth unity gain amplifier 11 drives the output load, which is presumed to be a capacitively loaded transmission line. The digital input to the output buffer 10 is provided to a square-to-ramp converter circuit 12, which converts the digital input to a slew-controlled ramp signal that is fed to the high bandwidth amplifier 11. The rise/fall time of the buffer output signal is controlled by the slope of the ramp generated. A bias circuit 14 provides a bias signal BIAS that is used by the converter circuit 12 to maintain constant slope on the ramp signal despite normal variations in the IC fabrication process, which provides for process-independent rise time with minimum ground/supply bounce.

Although Figure 1 shows a single bias circuit 14 providing bias for a single buffer output, the bias signal BIAS may be shared among multiple buffer outputs if such is desirable. In one embodiment, 26 individual buffers appear on a single integrated circuit, and in such an embodiment it is desirable to utilize six separate bias circuits 14, four providing bias to 16 of the buffers and two providing bias to the remaining 10 buffers.

Figure 2 shows the amplifier 11. The amplifier runs on a supply voltage of 3.3 volts, which can be generated from a 1.8 volt supply via a separate regulator (not shown). The amplifier 11 provides 1.8-volt low-voltage CMOS (LVCMOS) output signals. The amplifier 11 has a 250 MHz bandwidth to support a 120 Mbps data rate. Also the amplifier has a common mode range of 0 to 1.8V.

The amplifier 11 is a two-stage, Miller-compensated amplifier, which provides the desired high bandwidth with a reasonable gain. Since the amplifier 11 is internally compensated, the bandwidth is independent of the load capacitance. The first stage includes PMOS transistors Q1 and Q2 in a p-input folded cascode configuration, which helps in achieving an input common mode voltage of 0 volts and to ensure that the output reaches the desired VOL. The second stage of the amplifier 11 has a differential-to-single-ended configuration. The second stage is a class AB push-pull amplifier capable of actively sourcing and sinking load currents.

Figure 3 shows the ramp generator 12, which is operated from the 1.8 V supply AVDD. The ramp generator 12 converts the input data signal DATAZ to a process-independent ramp signal RAMPOUT, which is generated by switching on or off current sources that charge and discharge a capacitor C1. The switching action is achieved by transistors Q3 and Q4. Transistors Q5 and Q6 form the output transistors of the current sources. The currents supplied by the current sources, and therefore the respective slopes (rising and falling) of the ramp signal RAMPOUT, are controlled by the input signal BIAS from the bias circuit 14. As mentioned above, the signal BIAS is generated such that the slopes are substantially constant despite normal circuit variations caused by variations in the IC manufacturing process.

The bias circuit 14 is shown in Figure 4. This circuit takes a reference voltage signal BGREF of 1.2V and forces it on an internal circuit node labeled OUT. The circuit utilizes a reference current IREF that is generated using a band-gap reference and resistor of known value (not shown). The node OUT has a switched capacitor resistor to ground, which is formed by transistors Q7 and Q8 and capacitor C0. The effective resistance to ground is 1/CF, where C is the capacitance of C0 and F is the switching frequency, which is established by the clock signal CLK and its inverse CLKZ. Hence, the average current through the resistor is 1.2*CF. This current is mirrored to generate the bias signal BIAS. Note that capacitor C0 mirrors the input capacitance of the main amplifier. Thus, as the input capacitance varies with process, the current available to generate the ramp signal RAMPOUT varies proportionally, so that the slope stays substantially constant. One additional advantage of this scheme is that the current generated is proportional to the frequency of operation. Thus the ramp is slowed down at lower frequencies of operation. This gives lower ground bounce at lower operating frequencies.

One of the major contributors to ground and supply bounce is the transmission line that needs to be driven by the output buffer 10. In addition to the normal CV/t current that is required to charge the load capacitor, the output buffer also needs to provide the extra current required to overcome reflections arising because of non-terminated transmission line. In the illustrated embodiment, the output buffer can drive a 50 ohm transmission line that has 400 picoseconds delay time and is terminated with a 4 pf capacitive load. In experimental observations, the current that is sourced/sunk by the output buffer is four times the current required without the transmission line. This extra current must pass through the supply/ground inductance, and therefore can result in a big increase in the supply/ground bounce. This noise can be reduced by using a series termination resistor. This resistor absorbs the reflections coming from the load-end of the transmission line. As a result, the output buffer does not see the reflections of the transmission line. This reduces the current the buffer has to source/sink, thus giving a lower supply/ground bounce.

Figure 5 shows an evaluation circuit used for simulations to evaluate the performance of the above-described output buffer 10 when driving a 400-picosecond transmission line TL and a 4-pf load capacitor Cload. The inductance and resistance of the buffer output pin are shown as Lop and Rop respectively. The output buffer is assumed to be part of an integrated circuit having 26 outputs all driven by similar output buffers 10. The IC is assumed to have 10 ground pins and 8 supply pins, each of which is assumed to have 8 nH of inductance. This includes the self-inductance and the sum of mutual inductances from other pins. Two consecutive ground or supply pins are treated as a single pin to account for the large mutual inductance between them. These various inductances are included in the inductors Lpwr and Lgnd.

Another aspect that is taken into consideration is the effective series resistance (ESR) of the supply capacitors. Each data line of the output buffer has a capacitance of 60pf. Most of the switching current is provided by this capacitor and hence the ESR of this capacitor is very critical. The simulations assume a 2 ohm resistance in series with the 60pf capacitance to account for the ESR. This capacitor also reduces the effective ground inductance to the parallel combination of ground and supply inductance. These resistances are included in the resistors Rpwr and Rgnd.

The worst-case noise occurs in the strong process corner with maximum load capacitance. As shown in Figure 6, the worst-case ground bounce is less than 475mV. This is the bounce observed when all the 26 output buffers are switching in the same direction. A consecutive "10" pattern was observed not to be the worst-case switching pattern. Instead, a few 0's followed by a single 1 and a few 1's followed by a single zero provided the worst switching noise. The buffer output with this pattern is worth observing in order to verify whether the output voltage reaches VOL and VOH with sufficient margins. Another aspect that needs to be observed is the effect of 25 buffers switching together in one direction on the 26th buffer switching in the other direction. The average current consumed by the IC when all 26 buffers are switching at 120 Mbps is 200mA. The 10% to 90% rise time observed in simulation is 3 nS.

GROUNDS OF REJECTION

The three issues on appeal are first whether Claims 1 and 3 are anticipated by Jordan under 35 U.S.C. § 102(b); secondly whether Claims 1 and 3 are anticipated by Stuebing under 35 U.S.C. § 102(b); and thirdly whether Claim 3 is unpatentable over Jordan or Stuebing under 35 U.S.C. § 103.

ARGUMENTS

It is respectfully submitted that Stuebing does not disclose or suggest the presently claimed invention including the ramp signal having a slope determined by the bias current and an input capacitance of the analog amplifier.

Stuebing discloses that the control bus 14 ultimately controls the slope of the ramp generator 20. As a consequence; the amplifier 38 has nothing to do with such control. The Examiner alleges that this makes no sense with the presently claimed invention. The slope of the ramp generator is related to the characters of the amplifier, namely the bias current and input capacitance.

Since amplifier 38 has nothing to do with control of the ramp generator 20, there is no disclosure of the claimed subject matter.

Jordan does not disclose or suggest the presently claimed invention including the ramp signal having a slope determined by the bias current and an input capacitance of the analog amplifier.

The ramp generator 156 is controlled by slew rate compensator circuit 174 and has nothing to do with amplifiers 158 and 160 and consequently this reference could not meet the above mentioned claimed limitations.

Jordan '392 discloses at column 6, lines 20-25 that slew rate comparator 174 provides current I_1, I_2, and I_3 to ramp 1 and 2 generator 156 and to ramp 3 generator 162 and ramp 4 generator 164.

However, these currents do not depend in any way on comparators 156 and 160, since the current is provided from the slew rate compensators circuit 174 to the ramp generators.

Now the Examiner's attention is directed to column 5, lines 35-45 where Jordan '392 discloses that if an error occurs in ramps 1 and 2, 16 and 30, respectively, current 1_3 and I_2 are shifted from supplying ramp portion 90 and 92 to supply ramp portions 22 and 34 which in turn increases the slope of the ramps.

Consequently, the current I_2, I_3, and I_1 only depend on the error from the ramps and the comparators 160 and 158 do not influence the currents I_1, I_2, and I_3.

The claimed invention requires a ramp signal having a slope determined by the bias current and the input capacitance of the analog amplifier.

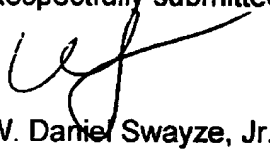
There is nothing in Jordan to disclose that the analog amplifier controls the ramp signal.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-5 under 35 U.S.C. § 102(b) and 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



W. Daniel Swayze, Jr.
Attorney for Appellants
Reg. No. 34,478

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-5633

APPENDIX

Claim 1 (previously presented): A low-noise buffer for a digital logic signal, comprising:

an analog amplifier;

a converter circuit operative to convert the digital logic signal to a ramp signal provided as an input to the analog amplifier, the ramp signal having a slope determined by a bias current and an input capacitance of the analog amplifier; and

a bias circuit operative to generate the bias current in a manner ensuring that the bias current varies as the input capacitance of the analog amplifier varies, such that the slope of the ramp signal remains substantially constant.

Claim 2 (original): A low-noise buffer according to claim 1, wherein the analog amplifier comprises:

an input stage including a differential pair of PMOS transistors in cascode configuration; and

a differential-to-single-ended, push-pull output stage.

Claim 3 (previously presented): A low-noise buffer according to claim 1, wherein the ramp circuit comprises a switched current source, the magnitude of the current supplied by the switched current source corresponding to the bias current.

Claim 4 (previously presented): A low-noise buffer for a digital logic signal, comprising:

an analog amplifier;

a converter circuit operative to convert the digital logic signal to a ramp signal provided as an input to the analog amplifier, the ramp signal having a slope determined by a bias current and an input capacitance of the analog amplifier; and

a bias circuit operative to generate the bias current in a manner ensuring that the bias current varies as the input capacitance of the analog amplifier varies, such that the slope of the ramp signal remains substantially constant,

wherein the ramp circuit comprises:

a first switched current mirror operative to generate current of one polarity when the digital logic signal has a first logic value; and

a second switched current mirror operative to generate current of the opposite polarity when the digital logic signal has a second logic value.

Claim 5 (previously presented): A low-noise buffer for a digital logic signal, comprising:

an analog amplifier;

a converter circuit operative to convert the digital logic signal to a ramp signal provided as an input to the analog amplifier, the ramp signal having a slope determined by a bias current and an input capacitance of the analog amplifier; and

a bias circuit operative to generate the bias current in a manner ensuring that the bias current varies as the input capacitance of the analog amplifier varies, such that the slope of the ramp signal remains substantially constant,

wherein the bias circuit comprises a switched-capacitor across which a predetermined reference voltage is placed to generate the bias current, the switched-capacitor including a capacitor having capacitance that varies as the input capacitance of the analog amplifier varies due to variations in the manufacturing process of the buffer.

EVIDENCE APPENDIX

Appellants are submitting no items of evidence.

RELATED PROCEEDINGS APPENDIX

Appellants have no submission for the Related Proceeding Appendix.